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| Date: 12 March 2021 | Course: CSE345 |
| Experiment 1 | Id: 2019-1-60-024 |
| Name: Adri Saha | Course instructor: Touhid Ahmed |

**Post Lab Report-01**

1. **2 Input XOR Gate**

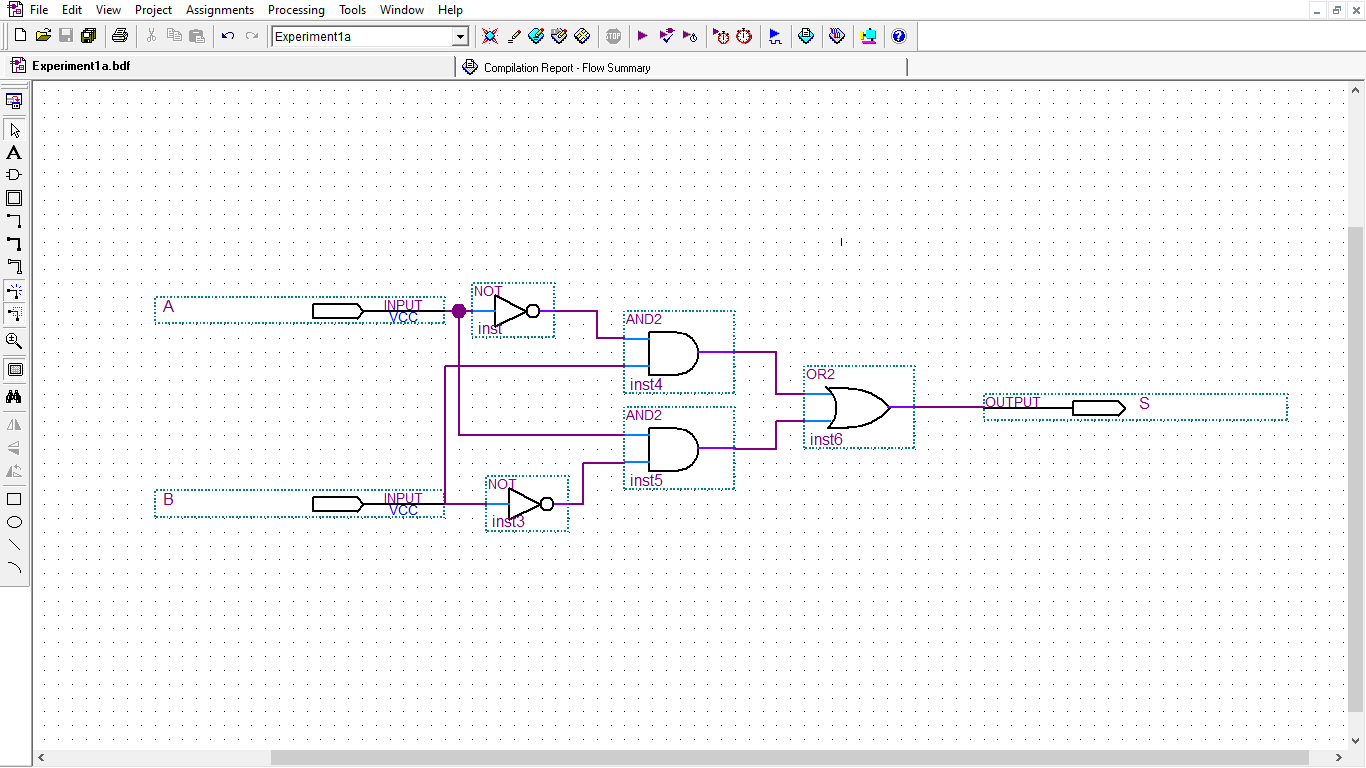
Here, A & B is input & output S

 Boolean expression is:

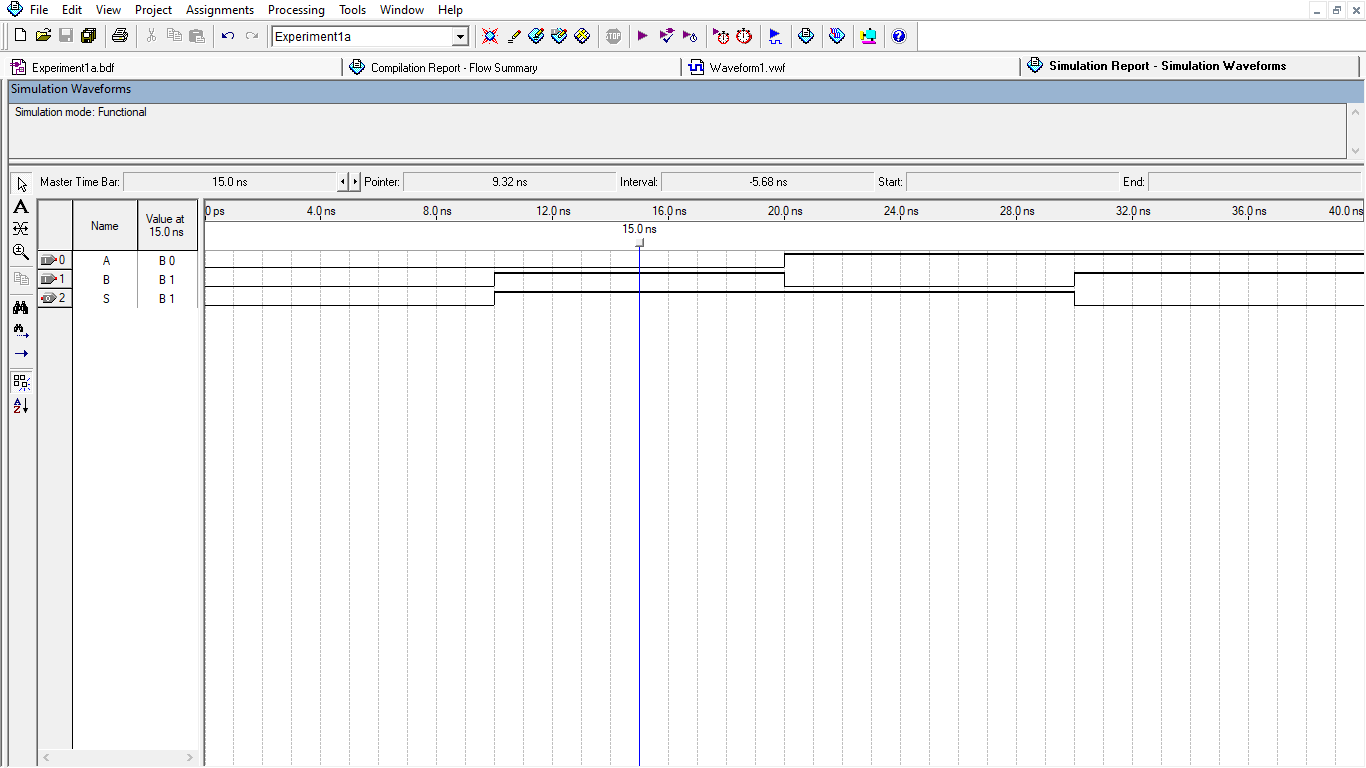
S = (A ⊕ B) = A.B⸍ + A⸍.B

**Schematic Circuit**:

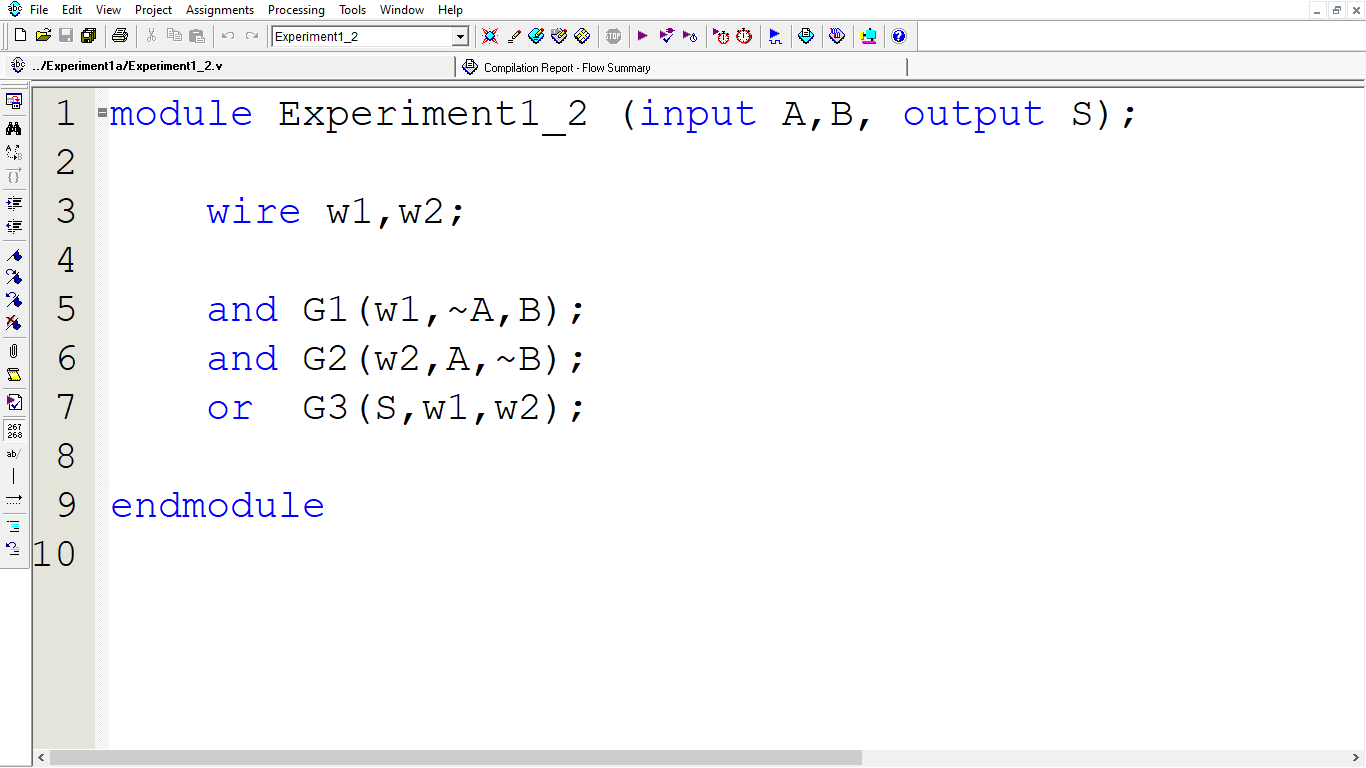




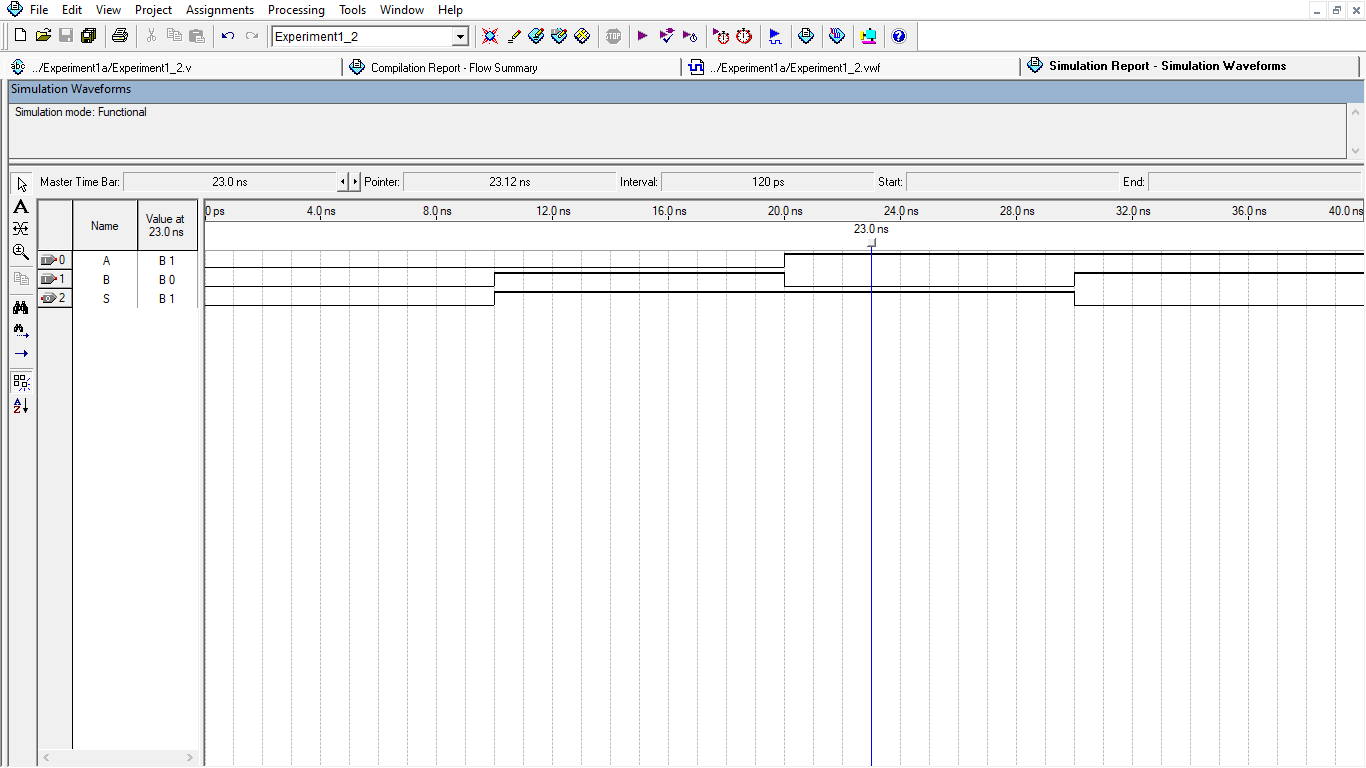
**Schematic Simulation:**



**Verilog Codes:**



**Verilog simulation:**

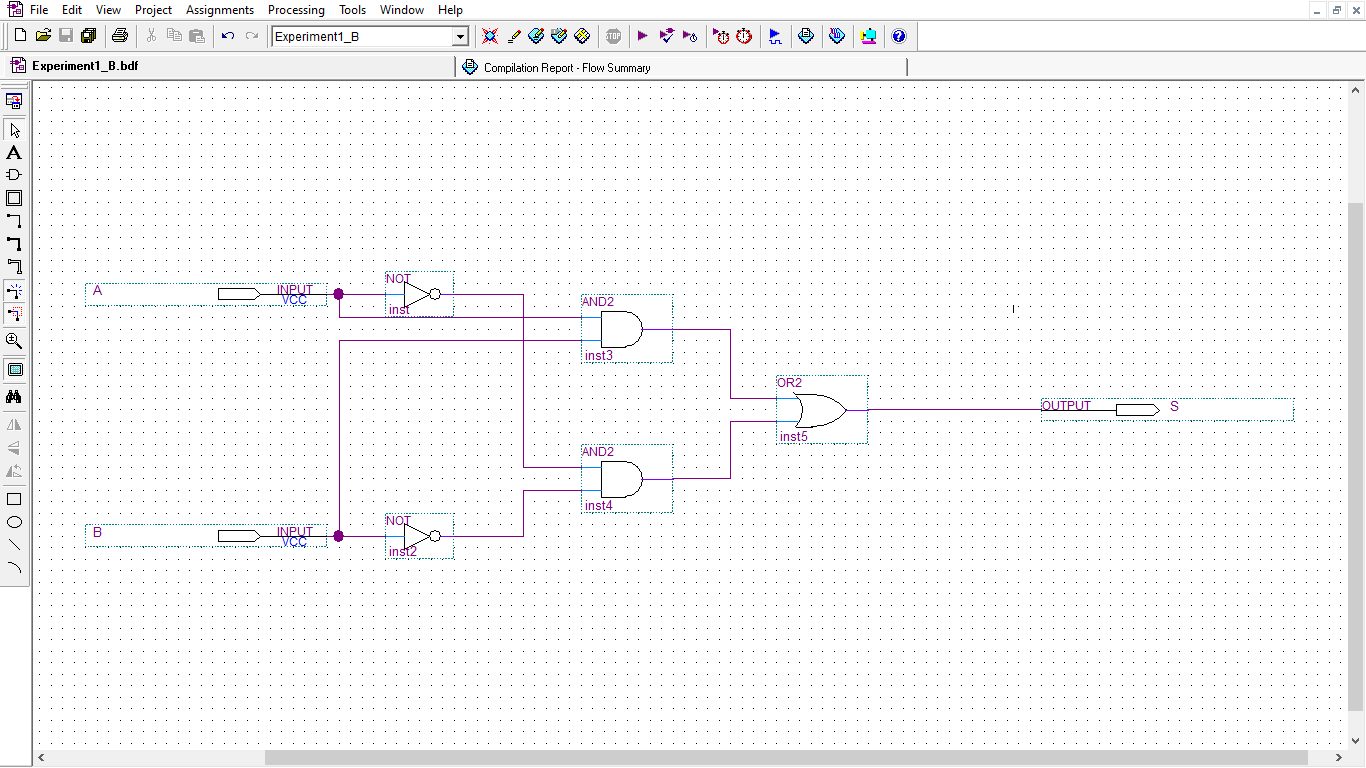


1. **2 Input XNOR Gate**

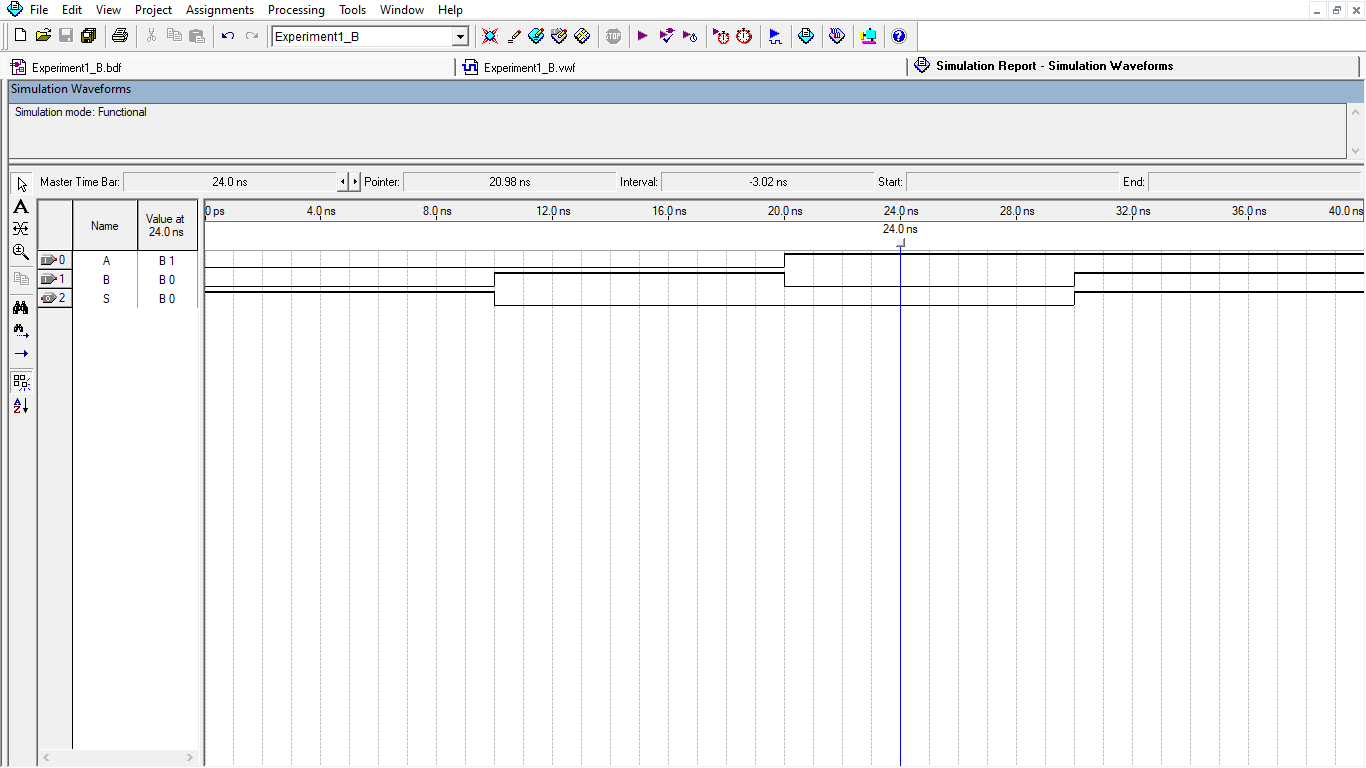
Boolean expression of 2 input exclusive nor gate: Q = (A ⊕ B) **= A⸍.B⸍ + A.B**

Schematic Circuit:

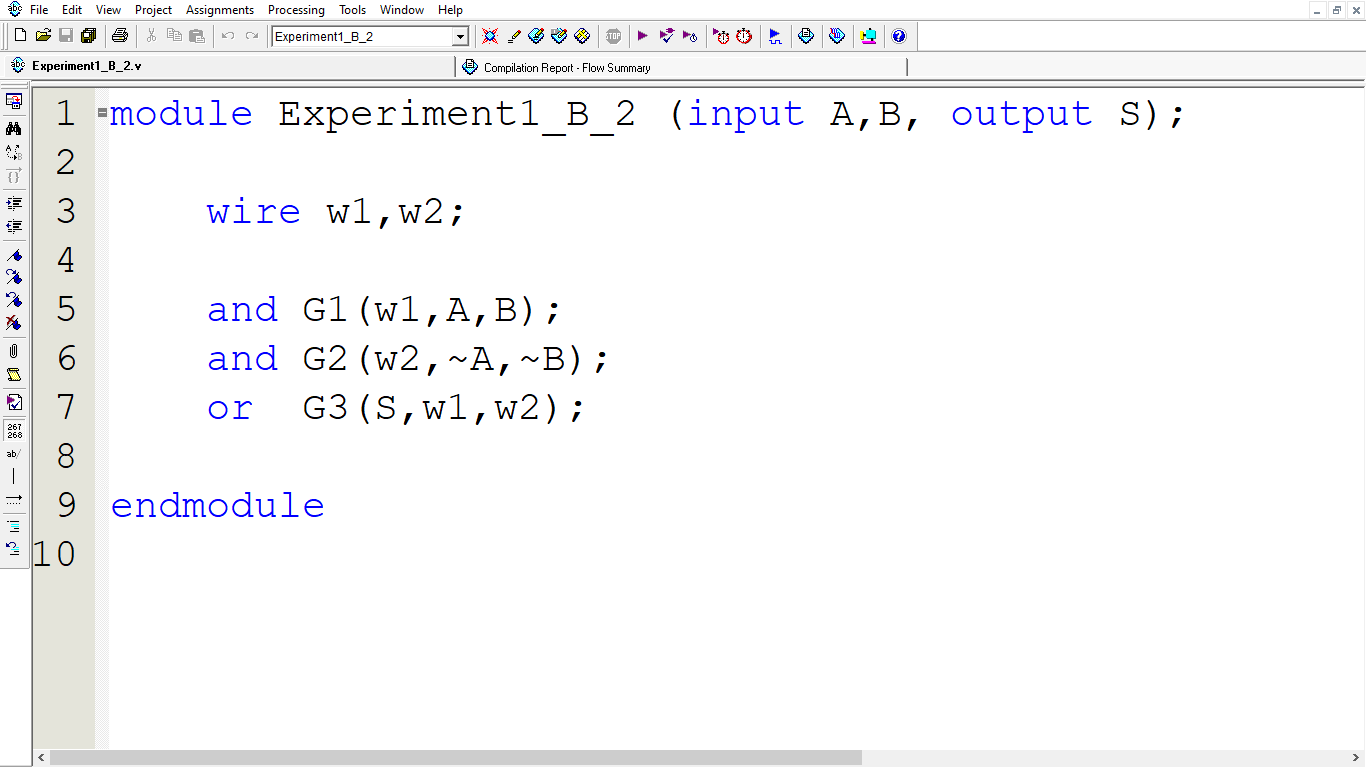




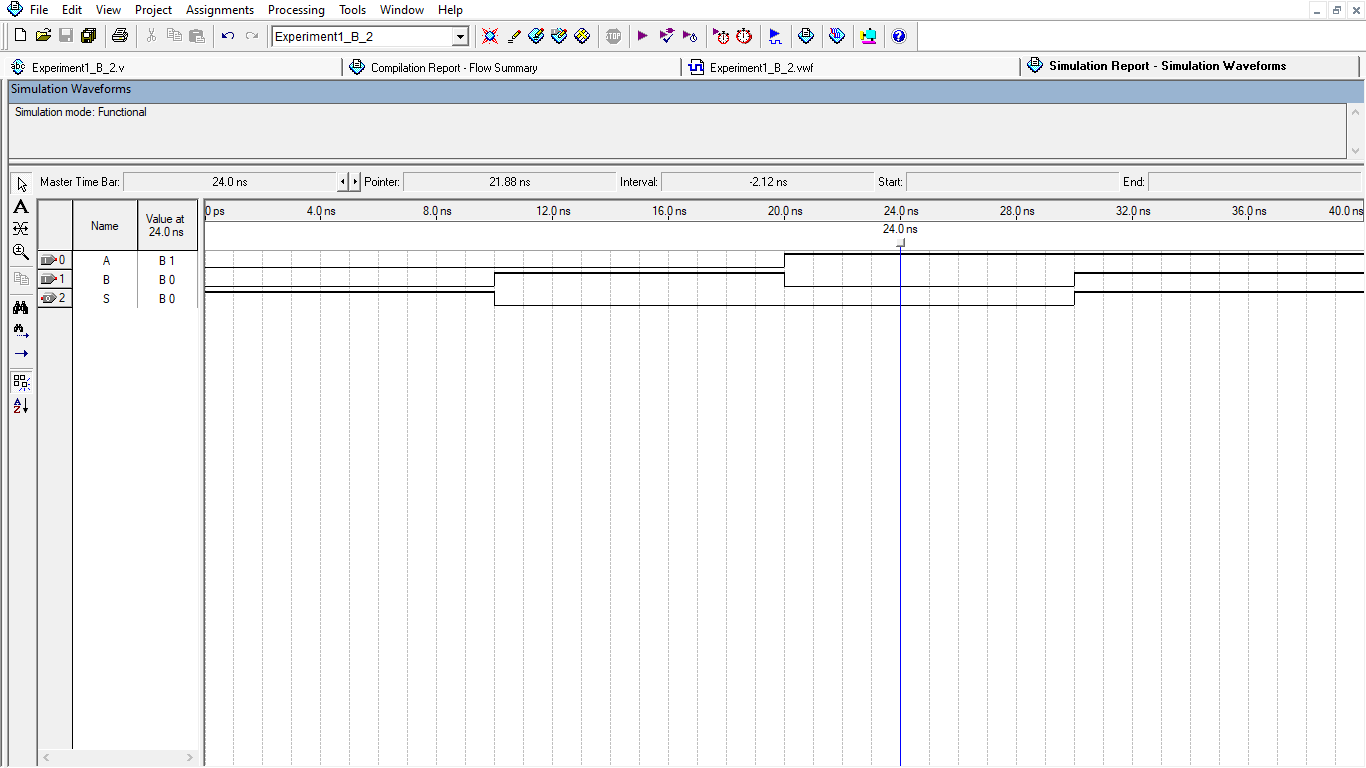
Simulation:



**Verilog Code:**



**Verilog Simulation:**

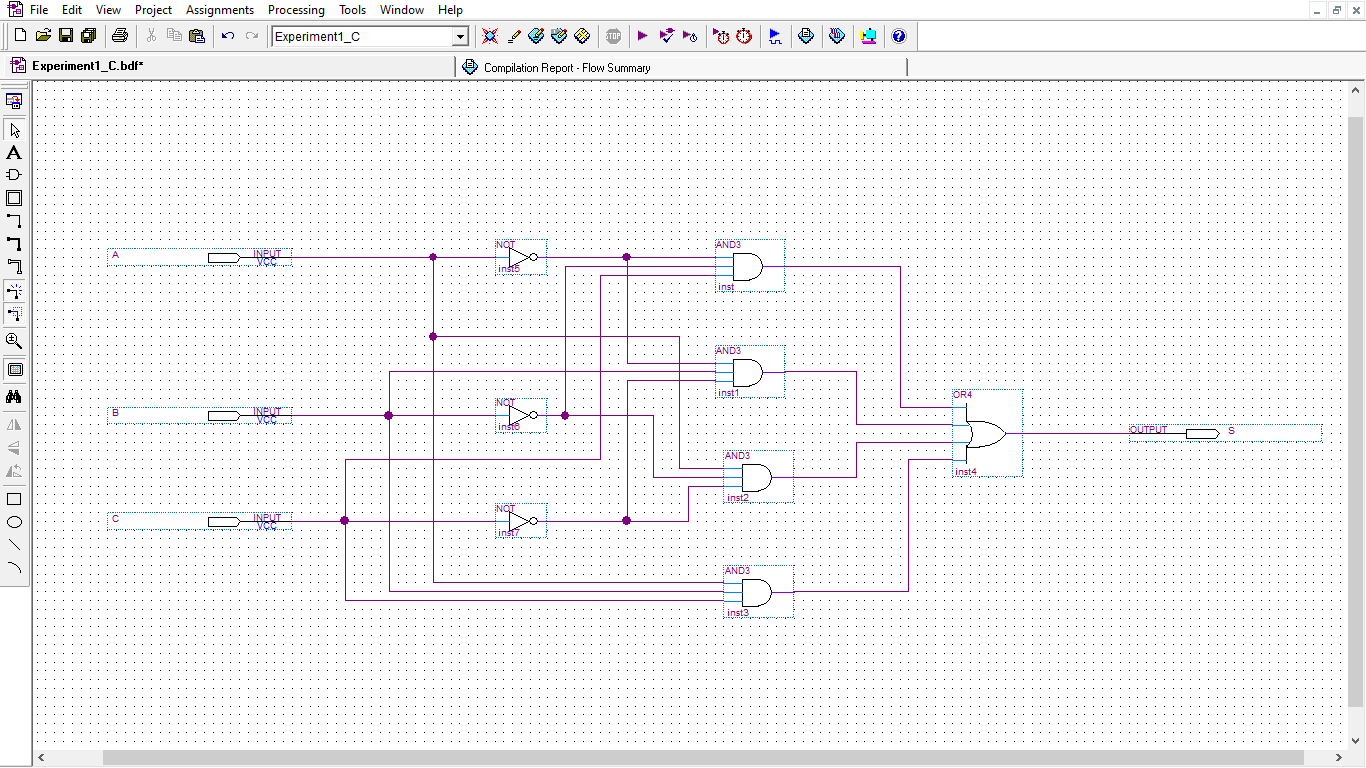


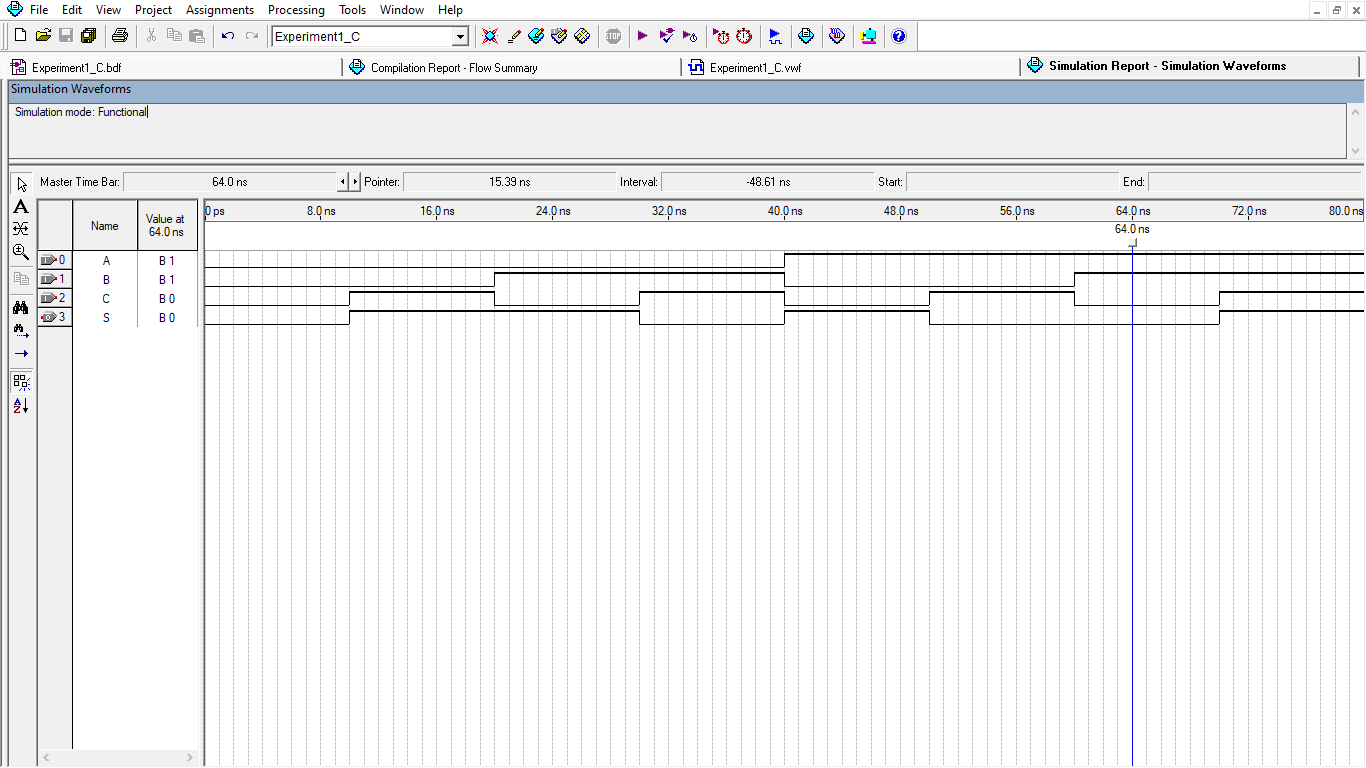
1. **3 Input XOR Gate**

Boolean expression**:  S = A⸍B⸍C + A⸍BC⸍ + AB⸍C⸍ + ABC**

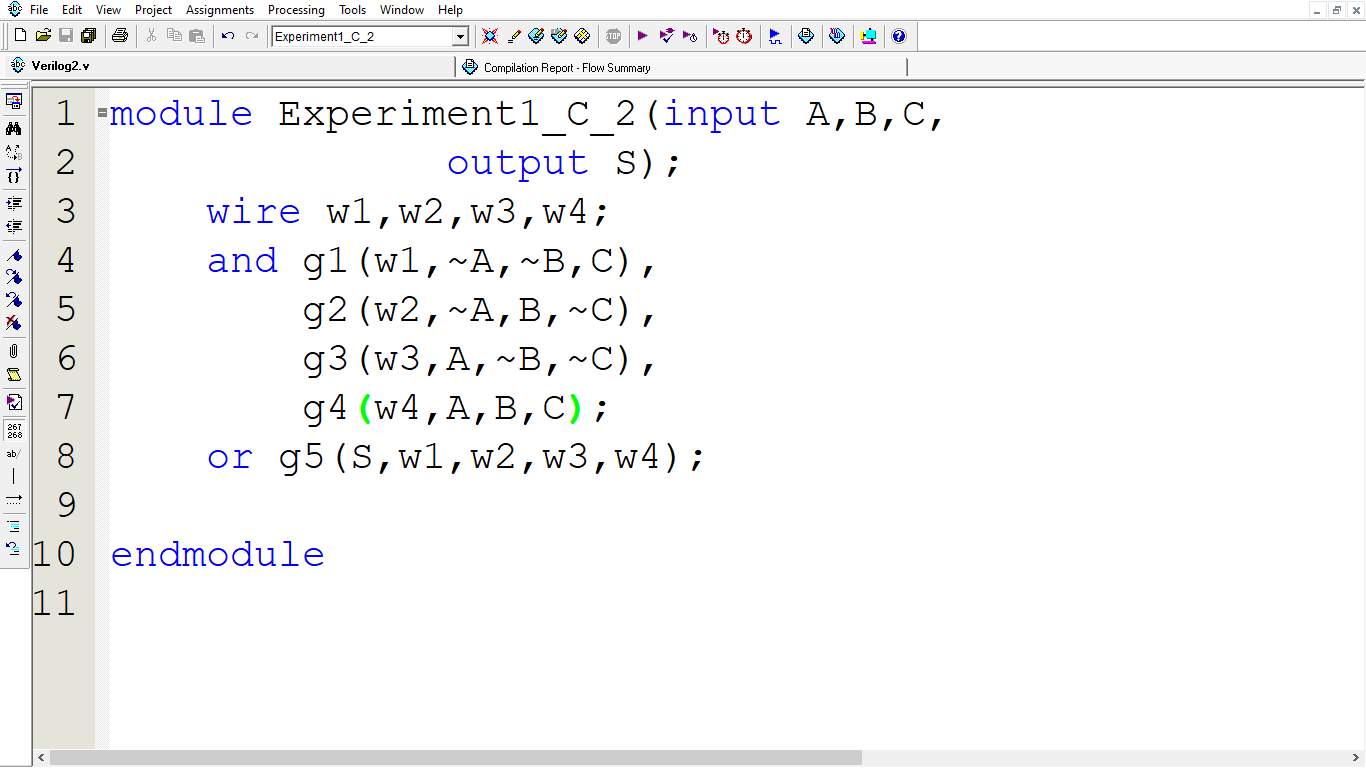
**Schematic Circuit:**

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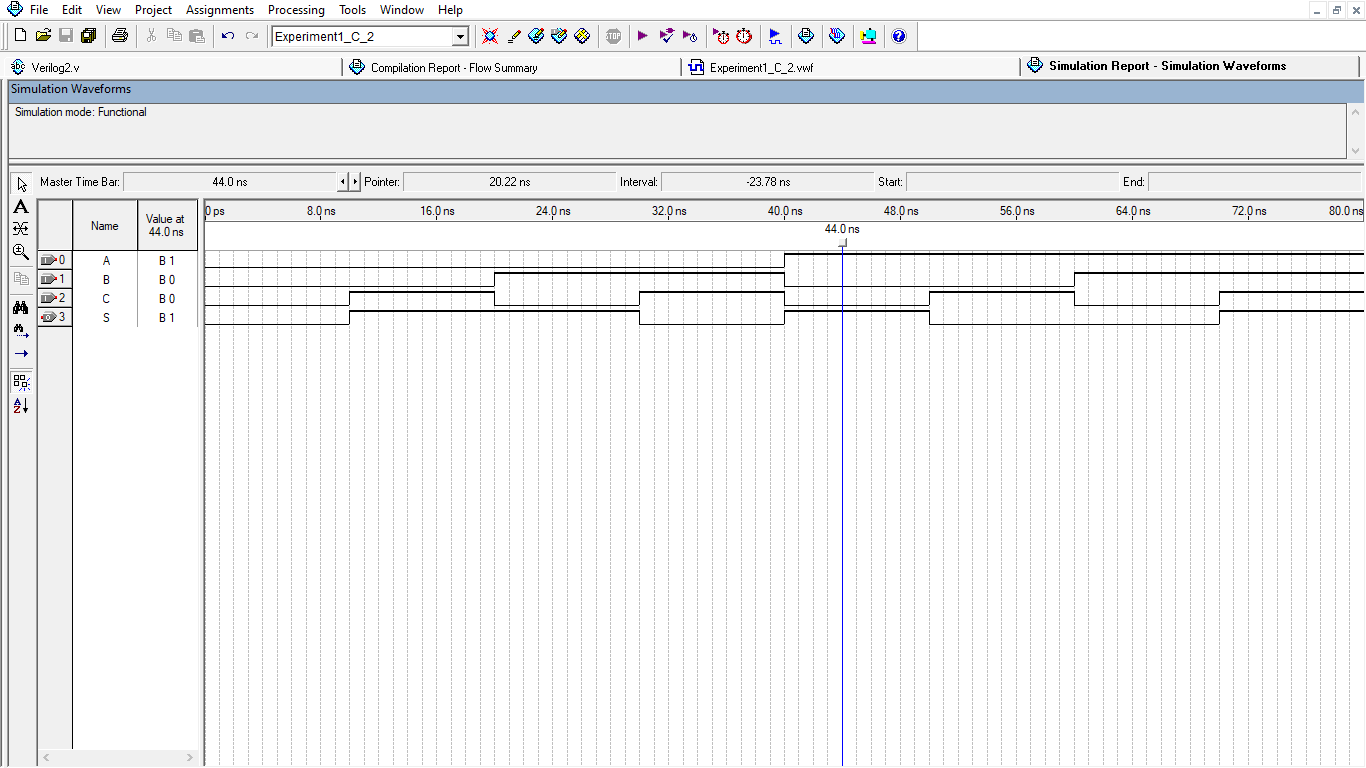




**Verilog Code:**



Verilog simulation:

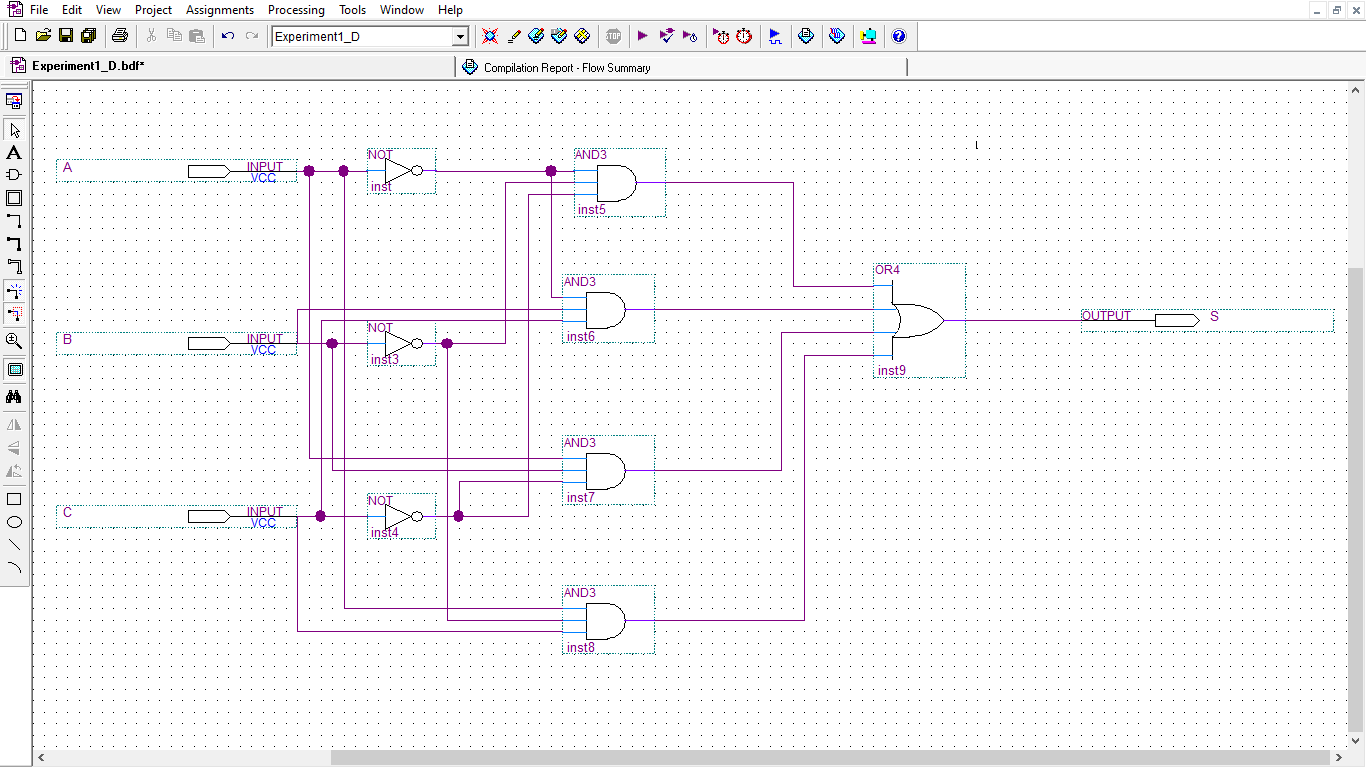


1. **3 Input XNOR Gate**:

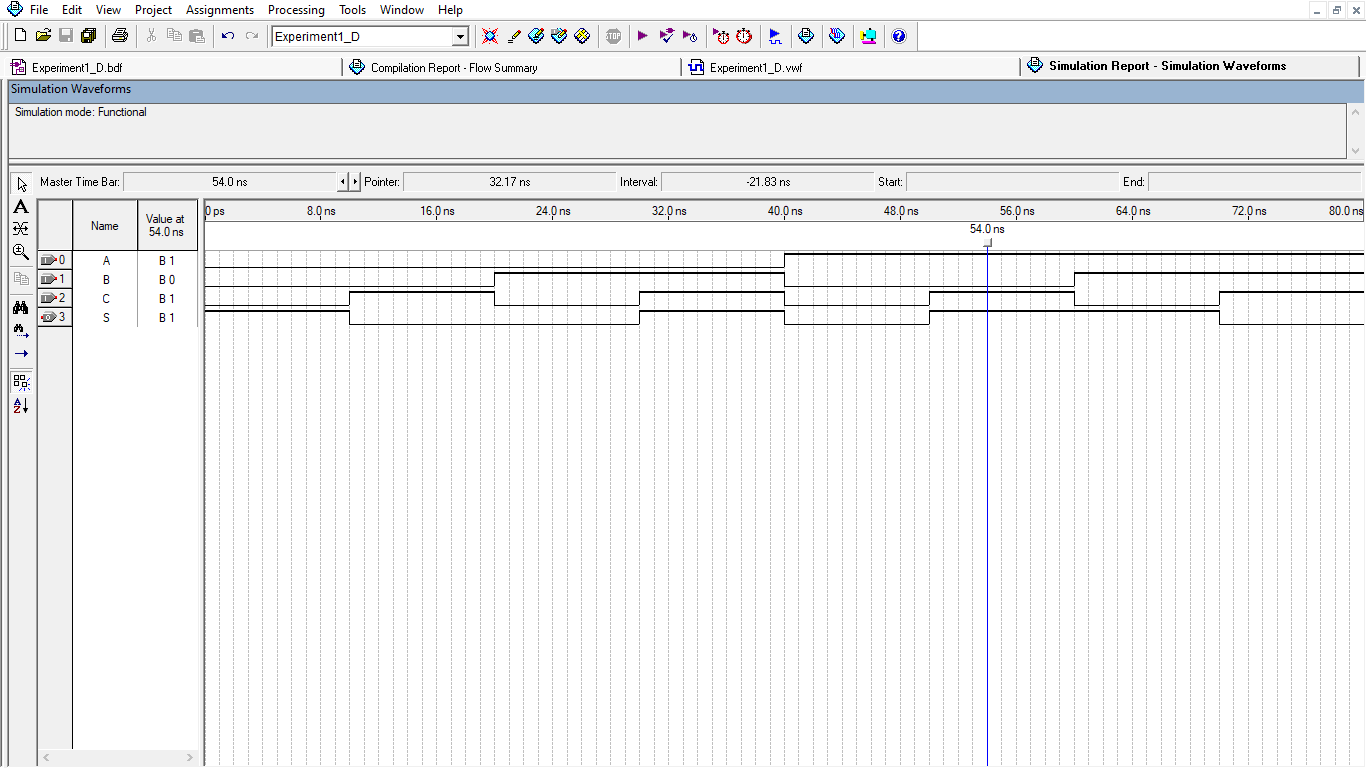
 Boolean expression of:  S = AB⸍C + ABC⸍ + A⸍BC + A⸍B⸍C⸍

Schematic Circuit:

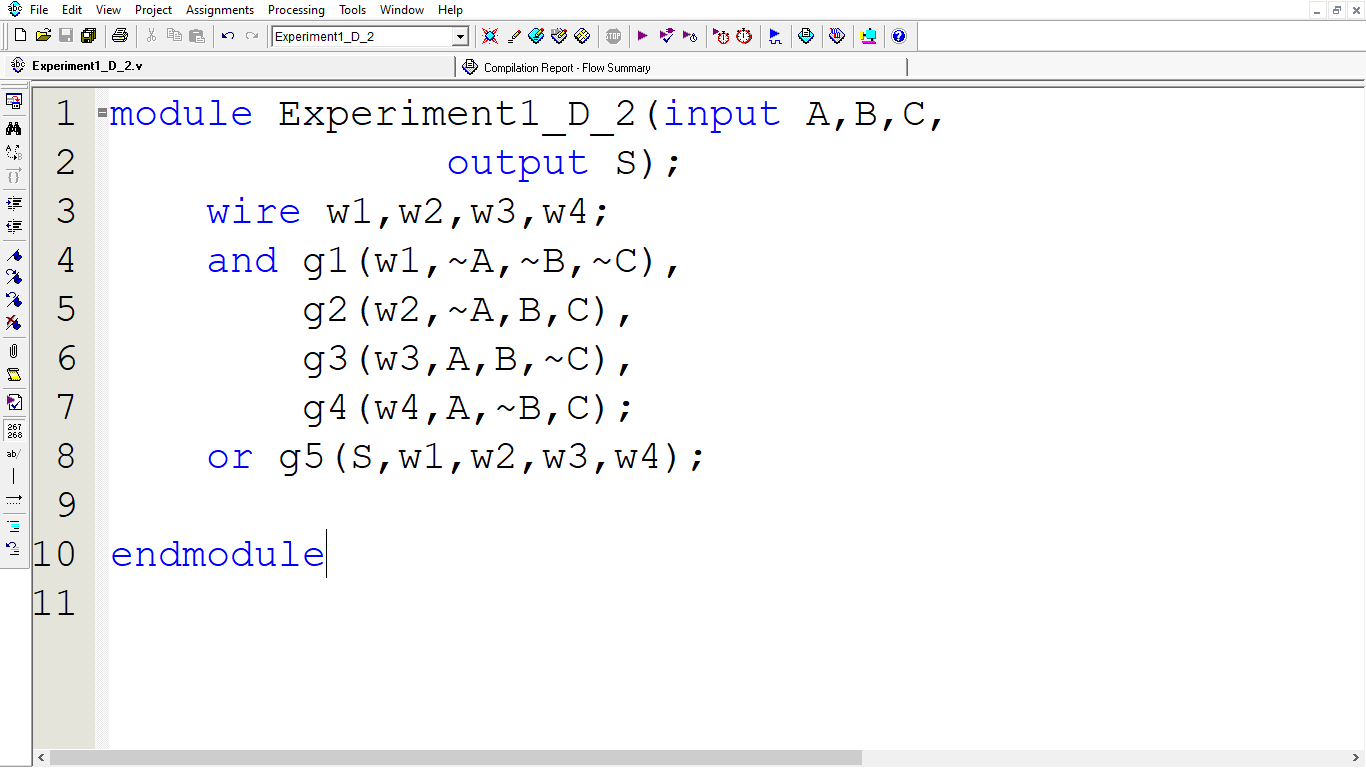




Schematic Simulation:



Verilog Code:



Verilog Simulation:

